

REMARKS

Claims 1-22 are pending in the present application.

In the Office Action, claims 17-22 were rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. In particular, the Examiner alleges that the specification does not state that the inserted zeroes comprise an equivalent time varying convolution code. Applicants respectfully disagree and note that the Patent Application describes a "zero code" comprising an equivalent time varying convolutional code at least in lines 13-16 on page 10 of the specification and in lines 1-5 on page 13 of the specification. The specification also describes inserting the zero code, contrary to the Examiner's allegations. See Patent Application, page 13, ll. 20-25. Applicants respectfully request that the Examiner's rejections of claims 17-22 under 35 U.S.C. § 112, first paragraph, be withdrawn.

In the Office Action, claims 1-22 were rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regard as the invention. Claim 1-22 were also rejected under 35 USC 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements. The Examiner's rejections are respectfully traversed.

First, the Examiner alleges that "forming an expanded digital input data sequence based on a constraint length" is indefinite since it is not clear how the constraint length is used to form the expanded digital input data sequence. Applicants respectfully disagree and note that inserting zeros expands the digital input data sequence. Furthermore, one embodiment of the present invention inserts one zero after each (K-1) information bits, where K is the constraint length. See Patent Application, page 12, ll. 11-12. Accordingly, Applicants respectfully submit

that the specification does describe forming an expanded digital input data sequence based on a constraint length.

In response to this argument, the Examiner alleges that a constraint length could be "almost any communication parameter that serves to constrain the communication system to a particular mode of operation." Applicants respectfully disagree and note that the constraint length of a convolutional encoder is defined in terms of the memory length and the code rate of the convolutional encoder. See Patent Application, page 13, ll. 13-16. Applicants therefore submit that the Examiner has adopted an improperly broad interpretation of the term "constraint length" that conflicts with the definition presented in the specification and the definition that would be applied by a person of ordinary skill in the art.

Second, the Examiner alleges that the specification does not state that the inserted zeroes comprise an equivalent time varying convolution code. Applicants respectfully disagree and note that the Patent Application describes a "zero code" comprising an equivalent time varying convolutional code at least in lines 13-16 on page 10 of the specification and in lines 1-5 on page 13 of the specification. Applicants further submit that a person of ordinary skill in the art having benefit of the present disclosure will appreciate that the zero code comprises one or more zeros.

For at least the aforementioned reasons, Applicants respectfully request that the Examiner's rejections of claims 1-22 under 35 U.S.C. § 112, second paragraph^h, be withdrawn.

In the Office Action, claims 10-22 were rejected under 35 USC 101 because the claimed invention is allegedly directed to non-statutory subject matter. In particular, the Examiner alleges that computer programs are non-statutory. Applicants respectfully disagree and note that a computer program is statutory material if it produces a "useful, concrete and tangible result." See MPEP §2106. Applicants respectfully submit that the method set forth in independent

claims 10 and 17 produces a useful, concrete and tangible result. In particular, the methods set forth in claims 10 and 17 produce a channel coded data stream. Furthermore, Applicants believe that the methods set forth in claims 10 and 17 fall under the safe harbor provided for processes that require measurements of physical objects or activities to be transformed outside of the computer into computer data. See MPEP §2106. In particular, claims 10 and 17 set forth receiving a digital input data sequence that may be representative of a physical activity performed outside of the computer. For example, the digital input data sequence may be representative of an acoustic signal provided to a microphone.

In response to this argument, the Examiner alleges that the claims are directed to non-statutory subject matter because two Examiners could, in principle, carry out the method using a pencil and paper. Applicants respectfully submit that whether or not the claimed invention could, in principle, be carried out by hand is irrelevant to determining whether or not the claims are directed to statutory subject matter. As stated above, the criterion for determining whether or not a method constitutes statutory subject matter is whether or not the method produces a "useful, concrete and tangible result." See MPEP §2106.

For at least the aforementioned reasons, Applicants respectfully submit that claims 10-22 are directed to statutory subject matter and request that the Examiner's rejections of claims 10-22 under 35 USC 101 be withdrawn.

In the Office Action, claims 1-22 were rejected under 35 U.S.C. § 102(b) as allegedly being obvious over Simanapalli (U.S. Patent No. 6,081,921) in view of Kato, et al (U.S. Patent No. 5,436,918). The Examiner's rejections are respectfully traversed.

With regard to independent claims 1, 10, and 17, Applicants describe and claim, among other things, periodically inserting known symbols into a digital input data sequence and forming

an expanded digital input data sequence based on a constraint length. By periodically inserting known symbols into the digital input data sequence and forming the expanded digital input data sequence based on a constraint length, the present invention may reduce the computational complexity of the channel coding system, may reduce the required memory storages, and may reduce the bit error rate. See Patent Application, page 7, ll. 16-25.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Simanapalli describes a convolutional encoder 22 that includes a bit insertion controller 28 which may interleave zero bits with input frame bits in an alternating manner. See Simanapalli, col. 3, ll. 3-18 and Figure 2. The Examiner alleges that inserting zero bits in an alternating manner is equivalent to forming an expanded digital input data sequence based on a constraint length of two. The Examiner also alleges that a constraint length could be "almost any communication parameter that serves to constrain the communication system to a particular mode of operation." Applicants respectfully disagree and submit that the Examiner has adopted an improperly broad interpretation of the term "constraint length" that conflicts with the definition presented in the specification and the definition that would be applied by a person of ordinary skill in the art. Applicants further note that Simanapalli has also defined the constraint length N in a manner consistent with the definition set forth in the present application and presented one conventional example in which the constraint length appears to be six. See Simanapalli, Figure 1 and related discussion.

As defined in the specification and in accordance with common usage in the art, the constraint length of a convolutional encoder is defined in terms of the memory length and the code rate of the convolutional encoder. See Patent Application, page 13, ll. 13-16. For example, a constraint length may be determined, in part, by a length of a register that receives input from a

receiving circuit. See Patent Application, page 11, ll. 13-16 and Figure 1. Thus, contrary to the Examiner's allegations, a constraint length cannot be "almost any communication parameter that serves to constrain the communication system to a particular mode of operation." In particular, simply inserting zero bits in an alternating manner, as described in Simanapalli, is not equivalent to forming an expanded digital input data sequence based on a constraint length of two. Accordingly, Applicants respectfully submit that Simanapalli is completely silent with regard to a constraint length of the convolutional encoder 22 and fails to teach or suggest forming an expanded input data sequence based on a constraint length.

The Examiner relies upon Kato to describe reducing a number of connections between trellis nodes in a trellis by inserting fixed bits in a bit stream. The fixed bits may be inserted near the central portion of encoding information bit data. In the case of inserting a plurality of bits, the bits may be inserted concentratedly or distributively. See Kato, col. 4, ll. 7-16 and Figures 5A-B. However, Kato is also completely silent with regard to a constraint length. Accordingly, Kato does not describe or suggest periodically inserting known symbols into a digital input data sequence and forming an expanded digital input data sequence based on a constraint length.

The cited references also fail provide any suggestion or motivation to modify the prior art to arrive at Applicants claimed invention. To the contrary, both of the cited references teach away from the Examiner's proposed modification of the prior art. Simanapalli appears to teach away from forming an expanded digital input data sequence based on a constraint length. In particular, Simanapalli describes interleaving zero bits with input frame bits in an alternating manner, e.g., inserting a zero bit after every input bit. However, the convolutional encoder described in Simanapalli appears to have a constraint length of six. See Simanapalli, Figure 1 and related discussion. Kato also teaches away from the present invention. In particular, Kato

teaches that fixed bits are inserted in a data stream to reduce a residual bit error ratio for the same line bit error ratio, whereas the present invention teaches periodically inserting known symbols to reduce the line bit error ratio. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not obvious over Simanapalli in view of Kato and request that the Examiner's rejections of claims 1-22 under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

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Respectfully submitted,


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